Claims:

1. A process for modifying the properties of a thin layer (1) formed on the surface of a support (2) forming a substrate (3) utilised in the field of microelectronics, nanoelectronics or microtechnology, nanotechnology, characterised in that it consists of:

- forming at least one thin layer (1) on a nanostructured support with specific upper surface (2),
- and treating the nanostructured support with specific upper surface (2) to generate internal strains in the support causing its deformation at least in the plane of the thin layer so as to ensure corresponding deformation of the thin layer to modify its properties.

2. The process as claimed in Claim 1, characterised in that it consists of treating the nanostructured support with specific upper surface (2) chemically to assure deformation corresponding to dilation or contraction of its nanostructure.

3. The process as claimed in Claim 1, characterised in that it consists of selecting a nanostructured support with a specific upper surface (2) among diverse nanostructures based on metals, semi-conductor or dielectric materials.

4. The process as claimed in Claim 1 or 2, characterised in that it consists of effecting the epitaxial growth of a crystalline material on the thin layer (1), after the treatment of the nanostructured support with specific upper surface (2).

5. The process as claimed in Claim 4, characterised in that it consists of selecting a thin layer (1) capable of possessing a

lattice parameter corresponding to the lattice parameter of the crystalline material to be formed by epitaxial growth on said thin layer (1) after treatment of the nanostructured support with specific upper surface (2).

6. The process as claimed in Claim 5, characterised in that it consists of forming a thin layer (1) prestrained or not on the nanostructured support with specific upper surface (2).

7. The process as claimed in Claim 1, characterised in that it consists of forming on the nanostructured support with specific upper surface (2), at least one intermediate layer (2_1) between the thin layer (1) and the nanostructured support with specific upper surface (2).

8. The process as claimed in Claims 4, 5 and 7, characterised in that it consists of forming on the thin layer (1) the epitaxial growth of a crystalline material selected from semi-conductor or superconductor materials.

9. The process as claimed in any one of Claims 1 to 3, characterised in that it consists of forming on the nanostructured support with specific upper surface (2) a thin layer (1) made of a material having piezoelectric properties.

10. The process as claimed in Claim 9, characterised in that it consists of performing on the thin layer (1) a lithographic operation to reveal piezoelectric zones (z).

11. The process as claimed in Claim 9 or 10, characterised in that it consists of deforming the nanostructured support with specific upper surface (2) so that electrical charges appear at the level of the thin layer.

12. A substrate for microelectronics, nanoelectronics or for microtechnology, nanotechnology, characterised in that it is formed by a nanostructured support with specific upper surface (2) and deformed following treatment and on the surface of which is formed at least one thin layer (1) deformed in correspondence with the support.

13. The substrate as claimed in Claim 12, characterised in that it comprises an epitaxial layer (4) of a semi-conductor or supra-conductor crystalline material, formed on the thin layer (1).

14. The substrate as claimed in Claim 12, characterised in that the thin layer (1) is made of a piezoelectric material.

15. Application of the substrate as claimed in Claim 12 to the production of an optoelectronic element.

16. Application of the substrate as claimed in Claim 12 to the production of an electronic component.